

Notice of References Cited	Application/Control No. 10/709,293		Applicant(s)/Patent Under Reexamination ALLEN ET AL.	
	Examiner Suchin Parihar		Art Unit 2825	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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*	B	US-2004/0096092	05-2004	Ikeda, Takahiro	382/141
*	C	US-2005/0108669	05-2005	Shibuya, Toshiyuki	716/009
*	D	US-2005/0021234	01-2005	Han, Dianli	702/013
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NON-PATENT DOCUMENTS

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	U	E. Papadopoulou and D. T. Lee, "Critical area computation via voronoi diagrams," IEEE Trans. Computer-Aided Design, vol. 18, pp. 463-474, Apr. 1999.
	V	[7] E. Papadopoulou, "Critical area computation for missing material defects in VLSI circuits," IEEE Trans. Semiconduct. Manufact., vol. 20, pp. 583-597, May 2001.
	W	E. Papadopoulou, D.T. Lee, "Critical Area Computation - A new Approach", Proc. International Symposium on Physical Design, April 1998, 89-94.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.